Type of Document	Document ID	Status
Technical Report	EPFL-PEL – EE-365 Report 1	Final Version
	Author(s) Name(s) Name1 Surname1 SCIPER ID Name2 Surname2 SCIPER ID	Function BSc Student(s)
	Assistant Name Israel Yepez López, Gaia Petrillo, Celia Hermoso Díaz	Date of Submission 15.03.2024

Title

R1: LLC RESONANT CONVERTER – BASIC DESIGN AND SIMULATIONS

Course Name

EE-365 Power Electronics

Keywords

LLC Converter, PLECS, Semiconductor

TABLE OF CONTENTS

LLC RESONANT CONVERTER SIZING

The first part of the project deals with sizing the main elements of a DC-DC LLC resonant converter, according to given converter specifications and design requirements. Fill out Table 1 with the parameters assigned to your group. Regarding the results of analytical calculations, please provide them with two digits after the decimal point in the unit provided in the solution box. Use the framed boxes below each question to insert your answers and explanations. Keep them concise.

Table 1 Given parameters and design requirements for the LLC Resonant converter.

Property	Value	Unit
$P_{out,nom}$	50	W
$U_{in,nom}$	45	V
$U_{in,min}$	40	V
$U_{in,max}$	50	V
U_{out}	24	V
$\Delta U_{out,pp,rel}$	5	%
f_{res}	160	kHz

-> Design requirements:

1. The converter should be designed to work at the resonant frequency at maximum input voltage.
2. The converter must be able to regulate the output voltage in the specified input voltage and power ranges.
3. The converter should always work in Zero Voltage Switching (ZVS) in the whole operating range.
4. Frequency operating range has to be within the limits $[0.5 \cdot f_{res}, f_{res}]$

Q1:TRANSFORMER TURN RATIO

At resonant frequency, the voltage gain $|M|$ equals unity, which represents one of the extreme operating points of your LLC converter. Design the transformer turns ratio to ensure that you can obtain the desired output voltage, whilst working at resonant frequency and operating with $U_{in,max}$.

$$n = \frac{V_{in,max}}{2 \cdot V_{out}} = \frac{50}{2 \cdot 24} = 1.04167$$

n = 1.04 / 2 pt.

Q2: MAXIMUM AND MINIMUM GAIN, M_{max}, M_{min}

To regulate the output voltage to a rated target value, while the input voltage may vary in the range [40, 50] V, the gain of the converter will vary between two values (M_{max} and M_{min}). Calculate the maximum and minimum required gain at the extreme values of the input voltage range.

$$M_{max} = 2 \cdot n \cdot \frac{V_{out}}{V_{in,min}} \quad , \quad M_{min} = 2 \cdot n \cdot \frac{V_{out}}{V_{in,max}}$$

M_{max} = 1.25 M_{min} = 1 / 4 pt.

Q3: INDUCTANCE RATIO, m

NOTE: You may have to iterate between Q3 and Q4 in case none of the Q curves of the previously chosen m satisfy the converter requirements.

Using the MATLAB script *EE-365_designLLC.m*, plot the normalized transfer function of the LLC converter for different inductance ratios. A recommendation is to start plotting from $m = 3$ and increase it by one until $m = 10$. Each one of these plots, for a fixed m value, considers a range of values for the quality factor Q. The operating range of the LLC resonant converter is limited by the peak gain (achievable maximum gain), which is indicated with $*$ in the plots provided in MATLAB.

Choose m that presents a suitable transfer function for your design operating frequency limits. Note that, your frequency operating range has to be within these limits and that the operating range of the converter is limited by the peak gain.
Include the gain curves plot of the selected inductance ratio and comment briefly why you have decided to choose it.

We are looking to get the maximal gain to occur as close as possible to the nearest frequency while staying on the right side of the peak. In order to achieve that, we selected m = 5 and Q = 0.4. We obtain an ideal curve with the largest frequency range and satisfying the other requirements: 10% margin and being on the right of the peak.

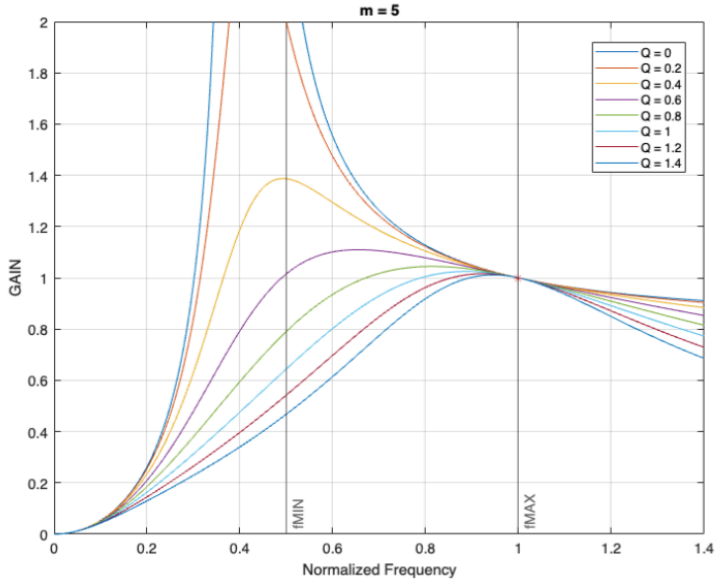


Figure 1 Voltage gain characteristics of the LLC resonant converter for $m = 5$

$m = 5$

/ 4 pt.

Q4: QUALITY FACTOR, *Q*

The output regulation range is determined by the gain, and by properly selecting Q and m according to the required specifications. The selected quality factor must cover both the maximum and minimum gain for the whole input voltage range to always guarantee the nominal output voltage and power. For practical purposes, the peak gain should be far enough away from the maximum gain (on the right side from the peak gain, on the gain curve), otherwise, ZVS could not be guaranteed due to deviations of parameters. For this reason, choosing a Q curve presenting a peak gain at least 10% above the maximum gain M_{max} required by your LLC converter is strongly recommended.

Choose a curve Q for the previously set m, that satisfies the minimum and maximum gain of your converter, taking into account the safe margin of at least 10% below the peak gain. Include the final gain curve plot for your design and comment briefly on why you have decided to choose it.

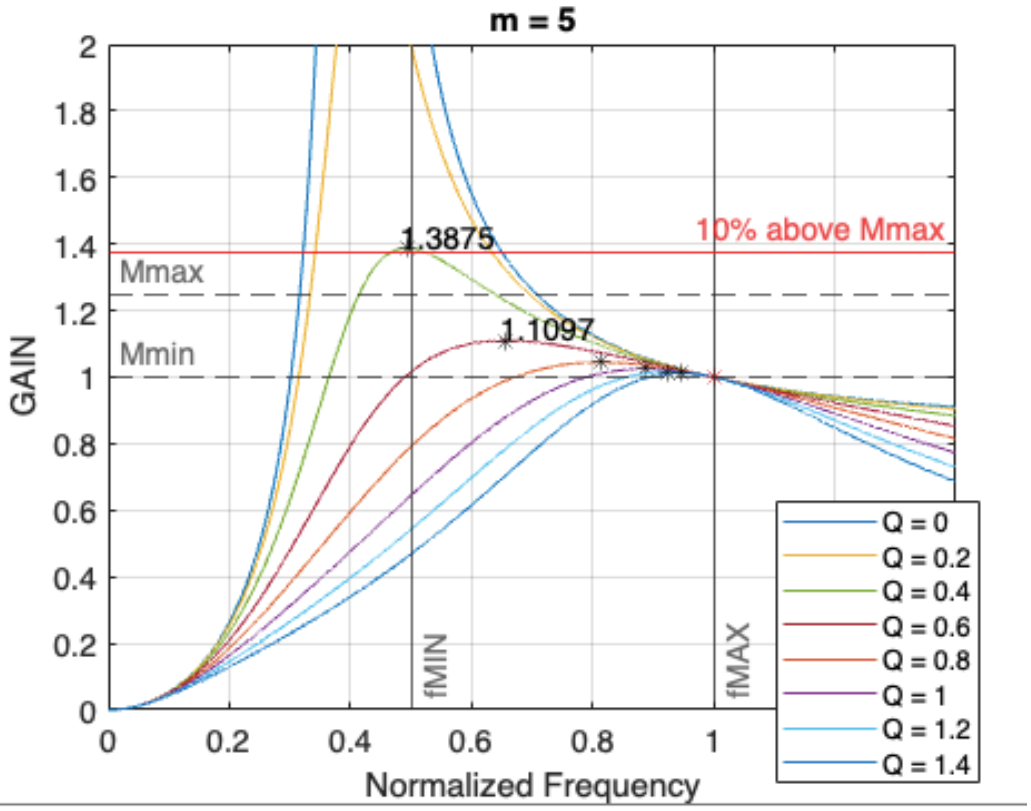


Figure 2 Voltage gain characteristics of the LLC resonant converter for $m = 5$

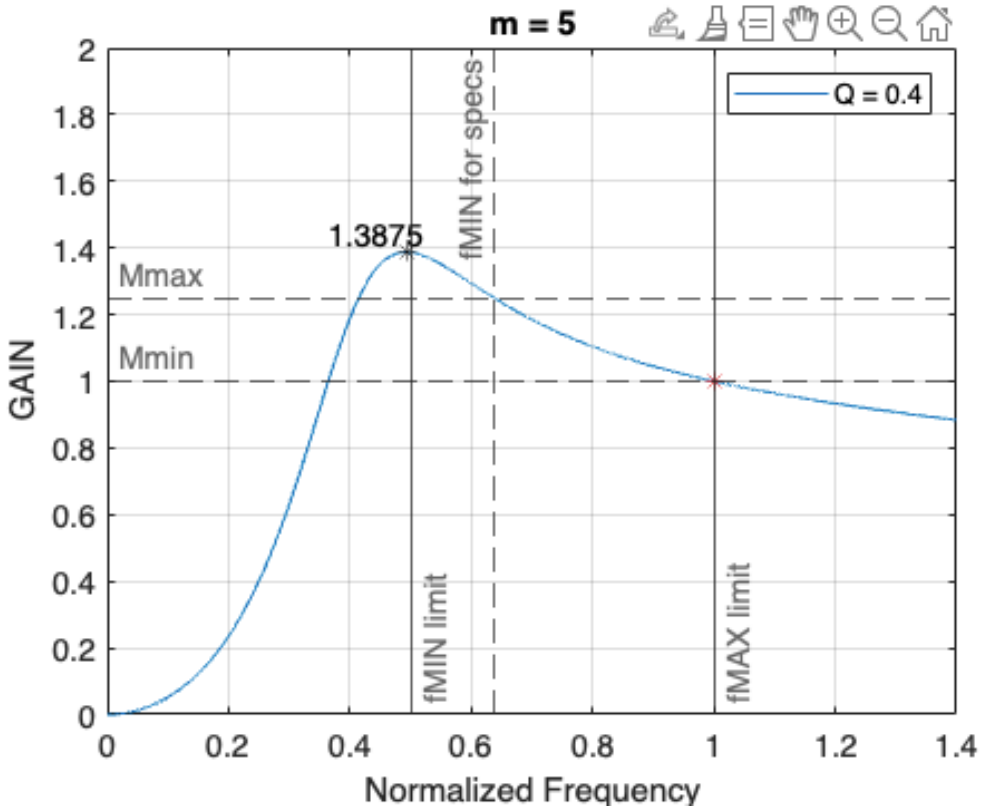


Figure 3 Voltage gain characteristic of the LLC resonant converter for $m = 5$ and $Q = 0.4$

$Q = 0.4$ / 4 pt.

Q5: EXTREME OPERATING POINTS

Based on the operating region you want your converter to work, choose the range of the normalized frequency where your design will operate correctly (x-axis of the given Matlab plots) and express the minimum and maximum normalized frequency. Remember that the operating frequency limits are $[0.5 \cdot f_{res}, f_{res}]$ and that the minimum switching frequency should be well limited above the peak gain frequency.

- Frequency (f_{nmax}) and gain (M_{min}) for no load condition.
- Frequency (f_{nmin}) and gain (M_{max}) for full load condition.

$f_{nmax} = 1$ $M_{min} = 1$ | $f_{nmin} = 0.637$ $M_{max} = 1.25$ / 4 pt.

Q6: DC LOAD, R_{dc} AND EFFECTIVE LOAD RESISTANCE, R_{ac}

First, calculate output resistance R_{dc} at nominal power. This is a simple resistive load that could be placed in the simulations in PLECS to validate your design. Secondly, utilizing the First Harmonic Approximation (FHA) and the LLC converter AC equivalent circuit, calculate the effective load resistance R_{ac}.

NOTE: Your design should have some margin for component tolerance. To guarantee control in case of unexpected load, please consider a 10% overload for the calculation of the output resistance as well as the effective load resistance.

$$R_{dc} = \frac{U_{out}^2}{1.1 \cdot P_{out,nom}} \quad , \quad R_{ac} = \frac{8n^2}{\pi^2} R_{dc}$$

$R_{ac} = 9.18\ \Omega$ | $R_{dc} = 10.47\ \Omega$ / 4 pt.

Q7: RESONANT CAPACITOR, C_r AND RESONANT INDUCTOR, L_r

Considering desired resonant frequency f_{res} (equation 1 and quality factor (equation 2, solve the corresponding equations and obtain the values for the resonant capacitance C_r and the resonant inductance L_r. For practical reasons, avoid having resonant inductance lower than 1.5µH.

$$f_{\text{res}} = \frac{1}{2\pi\sqrt{L_r \cdot C_r}} \tag{1}$$

$$Q = \sqrt{\frac{L_r}{C_r}} \cdot \frac{1}{R_{ac}} \tag{2}$$

$$C_r, L_r = \begin{cases} f_{\text{res}} = \frac{1}{2\pi\sqrt{L_r \cdot C_r}} \\ Q = \sqrt{\frac{L_r}{C_r}} \cdot \frac{1}{R_{ac}} \end{cases}$$

$C_r = 271nF$ $L_r = 3.65\mu H$ / 6 pt.

Q8: MAGNETIZING INDUCTANCE, L_m

With the value of L_r calculated, and with the known magnetizing ratio m, calculate the magnetizing inductance L_m.

$$L_m = m \cdot L_R$$

$L_m = 18.25\mu H$ / 1 pt.

Q9: OUTPUT CAPACITANCE, C_{out}

Using the provided PLECS model, find the required output capacitance C_{out} to fulfill the output voltage ripple requirements under the worst operating conditions.

The worst operating conditions are at V_{min} (40V) we then measure the capacitance in order to have an output voltage ripple$< 5\%$

$C_{out} = 80\mu\text{F}$ / 5 pt.

Q10: INPUT CAPACITANCE, C_{in}

Similar to the output capacitance, the input capacitance has to be calculated. Under nominal conditions, the input voltage must not drop below the minimum value in the event of a grid's outage.

Calculate the minimum required capacitance so that in case of a half-cycle grid's interruption (10 *ms*) the input voltage remains within the limits for a rated power condition. Consider the allowed input voltage drop from the rated value to the minimum value, during (10 *ms*).

$$\Delta E = \frac{1}{2}C_{in}V_{\text{nom}}^2 - \frac{1}{2}C_{in}V_{\text{min}}^2 \; ; \; \Delta E = P \cdot t \Rightarrow P \cdot t = \frac{1}{2}C_{in}(V_{\text{nom}}^2 - V_{\text{min}}^2) \Rightarrow C_{in} = \frac{2P}{V_{\text{nom}}^2 - V_{\text{min}}^2} \cdot 10 \cdot 10^{-3}$$

$C_{in} = 2.35m\text{F}$ /3 pt.

Q11: DISCHARGE RESISTANCE

Determine the required resistance $R_{discharge}$, in parallel to the input capacitor, to completely discharge the input capacitance from 100% to 5% of the rated voltage in less than 1 minute. This is needed for the safety reasons.

$$C_{in} = -\frac{10 \cdot 10^{-3}}{R_{discharge} \cdot \ln\left(\frac{V_{\text{min}}}{V_{\text{nom}}}\right)} \Rightarrow R_{discharge} = -\frac{10 \cdot 10^{-3}}{C_{in} \cdot \ln\left(\frac{V_{\text{min}}}{V_{\text{nom}}}\right)}$$

$R_{discharge} = 36.13\ \Omega$ /3 pt.

NOTE: For questions Q12, Q13 and Q14, show only three switching periods once the signals have reached their steady state.

Q12: PLECS VALIDATION FOR MAXIMUM INPUT VOLTAGE

Now that you have determined the resonant tank values, enter your parameters from Table 1 into the provided PLECS model of the LLC converter. Verify the results for maximum input voltage at resonant frequency and nominal output power through simulations. For this purpose, include the following waveforms:

a) Voltage across the resonant capacitor
b) Primary side input voltage
c) Current of the magnetizing inductance
d) Current of the resonant inductance
e) Secondary side diode current
f) Secondary side diode voltage
g) Output voltage

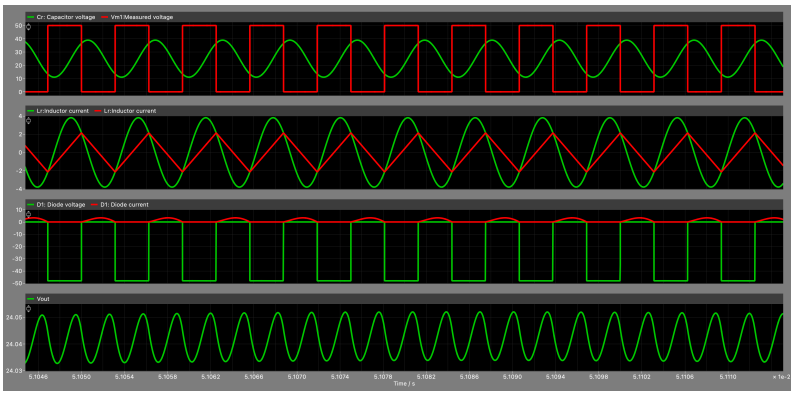


Figure 4 Voltage and current waveforms of interest. From top to bottom: resonant capacitor voltage V_{Cr} (t), input voltage of tank $U_{tank,in}$ (t), resonant inductance current I_{Lr} (t), magnetizing inductance current I_{Lm} (t), secondary side diode voltage U_D (t), secondary side diode current I_D (t), output voltage V_{out} (t); all as a function of time.

/ 3 pt.

Q13: PLECS VALIDATION FOR MINIMUM INPUT VOLTAGE

In Q12, you have validated that the converter operation is correct when the input voltage is maximum and the switching frequency is equal to the resonant frequency, in which the LLC converter is load-independent. Now, analyze the behavior of the converter when the input voltage drops to the minimum specified value. Verify through simulations, correct operation with minimum input voltage at the previously determined minimum frequency, with nominal output power. For this purpose, include the following waveforms:

a) Voltage across the resonant capacitor
b) Primary side input voltage
c) Current of the magnetizing inductance
d) Current of the resonant inductance
e) Secondary side diode current
f) Secondary side diode voltage
g) Output voltage

Additionally, from the scope, provide the measurement of output voltage ripple.

In Fig 5, we can see that the output voltage is too high. This is due to the fact that the FHA is correct at resonant frequency but becomes erronous, the further we move from it. So at minimum input voltage, the minimum frequency calculated (101.92 KHz) isn't right. By changing the value in PLECS, we foud that the actual minimum frequency was 115.25 KHz. In Figure 6, we can see that at the right frequency, the output voltage corresponds to the one expected.
Additionally, we find that the output voltage ripple is: $24.029 - 23.9856 = 0.0434$V

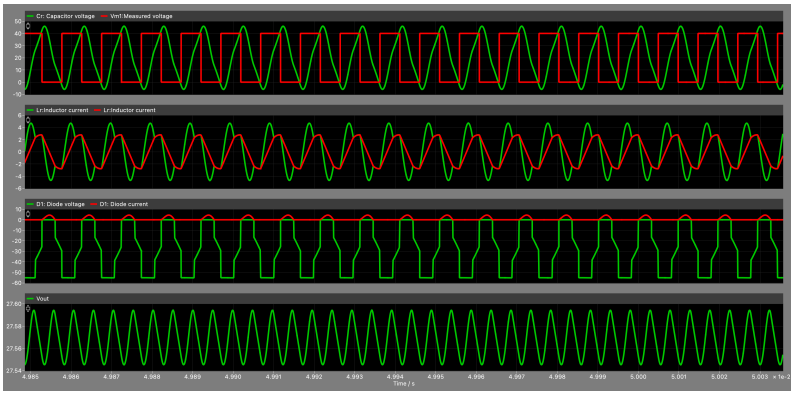


Figure 5 Voltage and current waveforms of interest. From top to bottom: resonant capacitor voltage $U_{Cr}(t)$, input voltage of tank $U_{tank,in}(t)$, resonant inductance current $I_{Lr}(t)$, magnetizing inductance current $I_{Lm}(t)$, secondary side diode voltage $U_D(t)$, secondary side diode current $I_D(t)$, output voltage $V_{out}(t)$; all as a function of time.

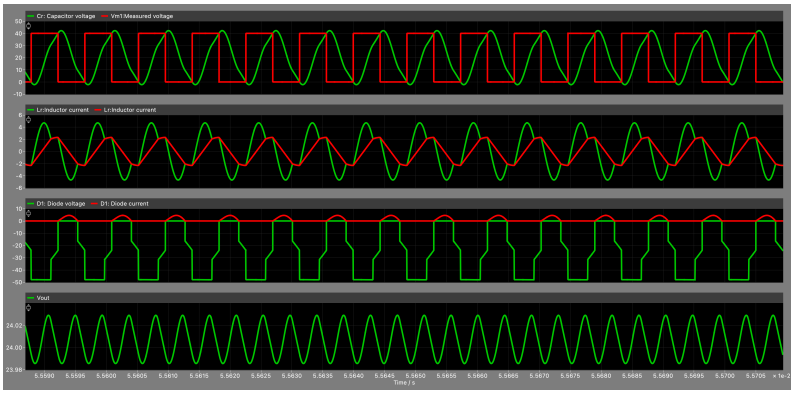


Figure 6 Voltage and current waveforms of interest. From top to bottom: resonant capacitor voltage $U_{Cr}(t)$, input voltage of tank $U_{tank,in}(t)$, resonant inductance current $I_{Lr}(t)$, magnetizing inductance current $I_{Lm}(t)$, secondary side diode voltage $U_D(t)$, secondary side diode current $I_D(t)$, output voltage $V_{out}(t)$; all as a function of time.

$\Delta U_{out,pp}\big|_{U_{in,min}} = 0.0434$V

/ 4 pt.

Q14: PLECS VALIDATION FOR 1/4 OF THE NOMINAL POWER

In Q13, you validated your LLC resonant converter design when the input voltage is at its minimum. In addition to the possible working operating points, the converter must be able to regulate the output voltage in specific voltage and power ranges. To validate that, analyze through simulation the results for minimum input voltage at the adequate frequency regulating 1/4 of the nominal power. For this purpose, include the following waveforms:

a) Voltage across the resonant capacitor
b) Primary side input voltage
c) Current of the magnetizing inductance
d) Current of the resonant inductance
e) Secondary side diode current
f) Secondary side diode voltage
g) Output voltage

Comment briefly your observations on the graphs.

At 1/4 of the nominal power (12.5W), minimum input voltage and the according minimum frequency (115.25KHz), we can see in Fig 7, that the ouput voltage becomes higher than the required one. This is due to the fact that changing the output power implies changing the RC, hence the value of Q. Here Q becomes lower and from Fig 2, we can see that it implies having a higher Q-curve which leads to a higher gain at the same frequency. So in order to reduce the output voltage to the required one, we need to increase the frequency (here to 118.08KHz).

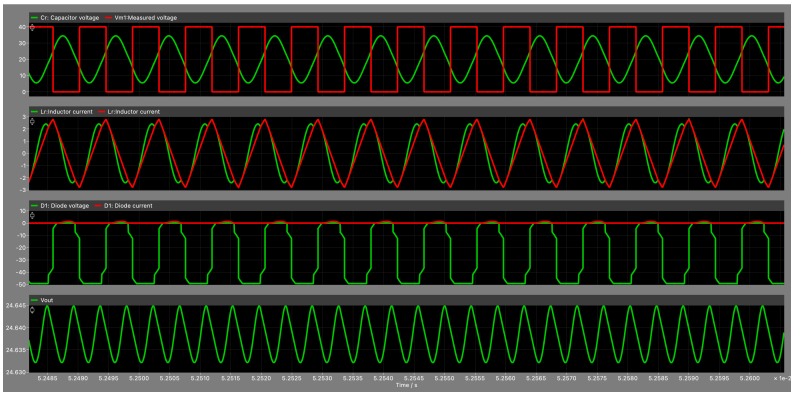


Figure 7 Voltage and current waveforms of interest. From top to bottom: resonant capacitor voltage U_{Cr} (t), input voltage of tank $U_{tank,in}$ (t), resonant inductance current I_{Lr} (t), magnetizing inductance current I_{Lm} (t), secondary side diode voltage U_D (t), secondary side diode current I_D (t), output voltage V_{out} (t); all as a function of time.

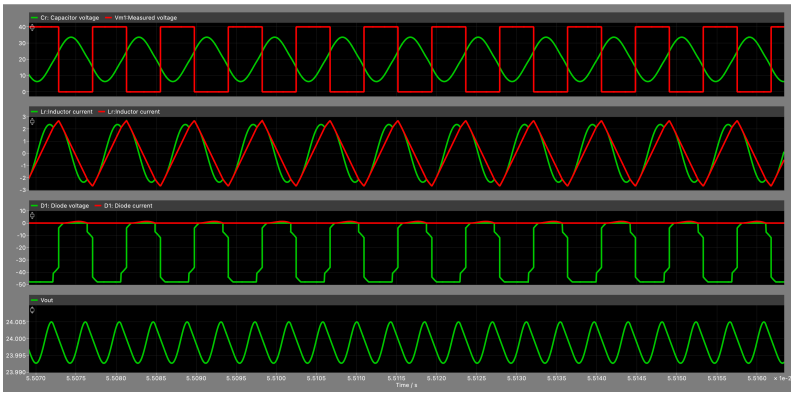


Figure 8 Voltage and current waveforms of interest. From top to bottom: resonant capacitor voltage U_{Cr} (t), input voltage of tank $U_{tank,in}$ (t), resonant inductance current I_{Lr} (t), magnetizing inductance current I_{Lm} (t), secondary side diode voltage U_D (t), secondary side diode current I_D (t), output voltage V_{out} (t); all as a function of time.

/ 4 pt.

Q15: EXPECTED GAIN VS SIMULATED GAIN

It is interesting to study the expected gain calculated utilizing the FHA (First Harmonic Approximation) against the gain obtained in the simulation in PLECS. Follow these steps to calculate the simulated gain:

- Choose a fixed input voltage with which you will carry out the upcoming simulations.
- From your the gain transfer function plot of your design, choose at least 5 operating frequencies within the operating range of your LLC resonant converter.
- Carry out a simulation per chosen frequency and obtain the average output voltage.
- Calculate the simulated gain of your LLC converter $M = 2n \cdot \frac{U_{out,PLECS}}{U_{dc,in}}$

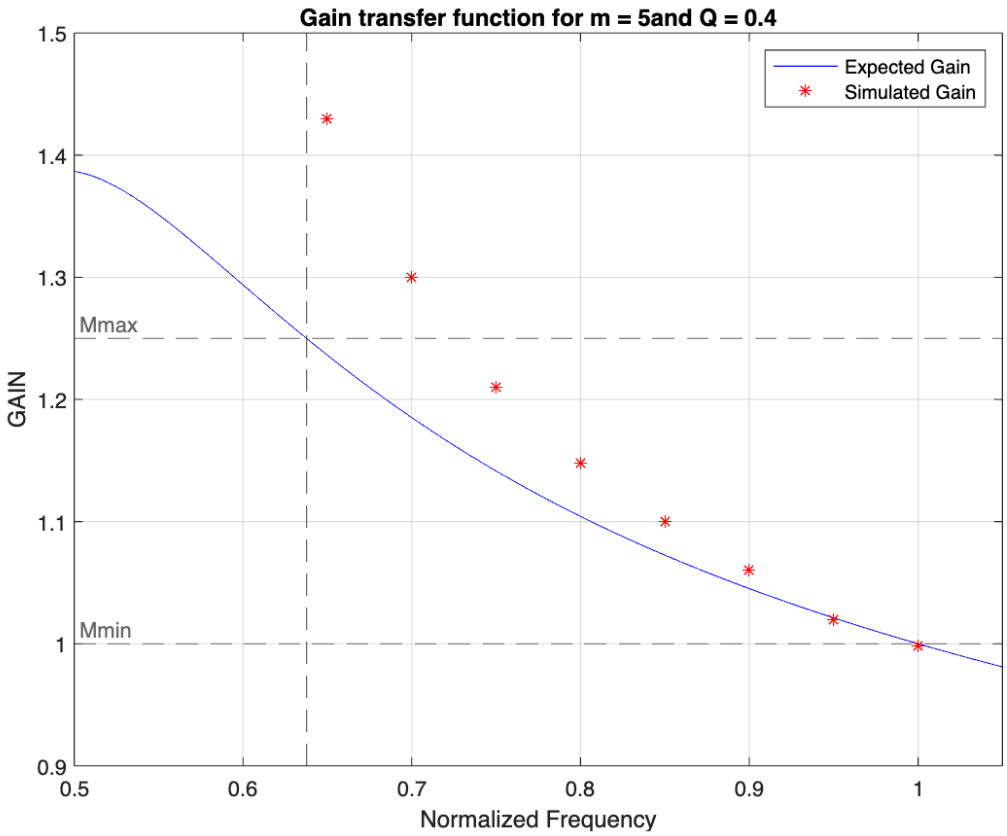


Figure 9 Ideal gain transfer function against simulated gain transfer function

We can see that the FHA is very close to reality at resonant frequency, but the further we move away from it, the bigger the error made by this approximation becomes. This is why we had to change our minimum switching frequency in Fig 6.

/ 5 pt.

SEMICONDUCTOR COMPONENTS

The second part of this report focuses on the selection of semiconductor devices for your design. You will have to derive equations for your design, eventually leading to the selection of proper semiconductors that you will use in your design. As in the first set of questions, provide numeric answers with a precision of two digits after the decimal point in the provided unit.

Q16: TRANSISTOR STRESSES

To select an appropriate transistor for your design, you need to determine the maximum voltage and current stress that it has to handle in your circuit under the worst-case conditions in the operation. For this purpose, provide:

a) The maximum voltage over the transistor $u_{T,max}$;
b) The maximum current flowing through the transistor $i_{T,max}$.

Parasitic effects cause voltage overshoots. Therefore, a good practice is to scale the maximal voltage stress with a factor of 1.5.

Obtain the maximal voltage stress and maximum current from PLECS simulations from the last section. In your answer, indicate the simulation result from which you obtained the results ($u_{T,max}$ and $i_{T,max}$) and then give a final answer for the maximum voltage stress by taking into account the factor.

$U_{T,max} = 50 \cdot 1.5 = 75\text{V}$

$i_{T,max} = 9.715\text{A}$

The highest voltage is obtained at $V_{in,max}$ and the highest current at $V_{in,min}$ (and f_{min})

$u_{T,max} = 75\text{V}$ | $i_{T,max} = 9.715\text{A}$ | / 4 pt.

Q17: DIODE STRESSES

Similarly to the previous question, to select the secondary side diodes, the maximum values of voltage and current must be identified. Thus, provide:

a) The maximum voltage over the diode $u_{D,max}$;
b) The maximum current flowing through the diode $i_{D,max}$.

Similar to Q16, obtain the maximal voltage stress and maximum current from PLECS simulations from the last section. In your answer, indicate the simulation result from which you obtained the results ($u_{T,max}$ and $i_{T,max}$) and then give a final answer for the maximum voltage stress by taking into account a factor of 1.5.

$u_{D,max} = 60 \cdot 1.5 = 90\text{V}$
$i_{D,max} = 7.5\text{A}$
The max voltage is obtained at $V_{in,max}$ and the max current at $V_{in,min}$ (and f_{max})

$u_{D,max} = 90\text{V}$ | $i_{D,max} = 7.5\text{A}$ | / 4 pt.

Q18: SEMICONDUCTOR SELECTION

Based on the obtained values from Q16 and Q17, select from the offered lists in Tables 2 and 3 a specific MOSFET (Metal Oxide Semiconductor Field-Effect Transistor) device and a specific diode for your design. Elaborate briefly why you chose exactly these two models and highlight them in the Tables, as it is exemplified for the first device.

Note that all devices are built in a TO-220 case, or variant, as shown in Fig. 10. Moreover, the package of the Schottky diodes is dual, therefore, you will only need to choose one piece for your design.

Given the parameters we just found, we chose the transistor nº2 and the diode nº3 as they both give a sufficiant margin without being excessive. The diode voltage U_{dc} is close to our $U_{D,max}$, but we already took a margin with a factor of 1.5 for parasitic effects.

MOSFET model No. : 2 | Diode model No. : 3 | / 6 pt.

Table 2 The list of offered MOSFET devices. The parameter U_{ds} is the rated drain-source voltage, whereas the I_{cont} stands for continuous drain-source current.

No.	Manufacturer	Product	U_{ds} (V)	I_{cont} @ 100 °C (A)	$R_{ds,on}$ @ 25 °C (mΩ)
1	Onsemi	FDPF390N15A	150	15	40
2	Nexperia	PSMN034-100PS	100	22	62 (@ 100 °C)
3	Onsemi	FDPF680N10T	100	7.6	68
4	Vishay	SIHF530-GE3	100	10	160
5	Vishay	IRF510PBF	100	4	540
6	Vishay	IRFI510GPBF	100	3.2	540
7	Vishay	IRFZ24PBF-BE3	60	12	100
8	Infineon	IRFZ24NPBF	55	12	70

Table 3 The list of offered Schottky diode devices. The parameter U_{dc} refers to the maximum dc blocking voltage, whereas I_{cont} is the continuous forward current.

No.	Manufacturer	Product	U_{dc} (V)	I_{cont} (A)	U_f @ 25 °C (mV)
1	Rohm	RB088T100NZC9	110	10	870
2	Vishay	MBR20100CTVI1	100	10	800
3	Rohm	RB205T-90NZC9	90	15	780
4	Rohm	RB085T-90NZC9	90	10	830
5	Rohm	RB095T-90NZC9	90	6	750
6	Rohm	RB205T-60NZC9	60	15	580
7	Rohm	RB095T-60NZC9	60	6	580
8	Vishay	VT3045C-M3/4W	45	30	570

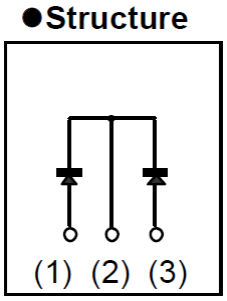


Figure 10 Schottky diode structure of devices listed in Table 3

CALCULATION OF CURRENT AVERAGE AND RMS VALUES

In this section, you will obtain the Average and the RMS (Root Mean Squared) current values of the LLC resonant converter through simulation. The results have to be given with two digits after the decimal point using the given unit.

Q19: PLECS SIMULATION

Using the provided PLECS model, consider worst-operating conditions, obtain the values for:

a) The transistor RMS current $I_{T,rms}$;
b) The transistor average current $I_{T,avg}$;
c) The diode RMS current $I_{D,rms}$;
d) The diode average current $I_{D,avg}$.

In your answer, indicate the simulation result from which you obtained the results $I_{T,rms}$, $I_{T,avg}$, $I_{D,rms}$, $I_{D,avg}$.

When V_{in} is modified, the current increases naturally, in order to maintain the same consumption of power. So the worst case conditions are when V_{in} and f_{sw} are minimum.

$I_{T,rms}$ = 2.14 A | $I_{T,avg}$ = 1.21 A | $I_{D,rms}$ = 1.97 A | $I_{D,avg}$ = 1.1 A | / 4 pt.

THERMAL DESIGN BASED ON THE EXPECTED SEMICONDUCTOR LOSSES

Based on your previous results, losses can be calculated and compared with the provided MATLAB Loss Tool. The results using the worst case (provided by the Loss Tool) will be used to select appropriate heatsinks for your design. As in the other questions, results should be given with two digits after the decimal point in the unit indicated. The Infineon Application Notes may serve you as a guideline for questions Q20, Q21 and Q22.

Q20: DIODE CONDUCTION LOSSES

Using the datasheet of your selected diode as well as the results from your simulations from Q19, calculate the diode conduction losses $P_{D,cond}$ at steady state under worst-operating conditions (f_{min} and $U_{in,min}$). Note that the datasheet values may not be at the temperature your diode will operate, which is assumed to be 135 °C.

$$P_{D,cond}\big|_{nom} = u_{D0} \cdot I_{av} + R_D \cdot I_{rms}^2$$

u_{D0} corresponds to the U_r of the diode at 135º, from the datasheets, we find it to be 450mV. From the slope in the datasheet, we also find $Rd = 0.2\Omega$.

$P_{D,cond}\big|_{nom} = 1.272$ W

/ 7 pt.

Q21: TRANSISTOR CONDUCTION LOSSES

Using the datasheet of your selected transistor as well as the results from your simulations from Q19, calculate the transistor conduction losses at steady state under worst-operating conditions (f_{min} and $U_{in,min}$). Identical to the diode, the transistor is assumed to operate at a temperature of 135 °C.

We use the same formula as above:

$$P_{T,cond}\big|_{nom} = u_{D0} \cdot I_{av} + R_{DSon} \cdot I_{rms}^2$$

For R_{DSon}, in the datasheet, we choose the value at the worst operating conditions (at 175º) which gives us $96m\Omega$. Since the MOSFET has no threshold voltage, we get $u_{D0} = 0$
Hence we get:

$$P_{T,cond}\big|_{nom} = R_{DSon} \cdot I_{rms}^2 = 0.44$$

$P_{T,cond}\big|_{nom} = 0.44$ W

/ 7 pt.

Q22: TRANSISTOR SWITCHING LOSSES

Using again the datasheet and your previous results, calculate the transistor turn-on and turn-off losses $P_{T,on}$, $P_{T,off}$, at steady state under worst case operating conditions, this is, the conditions resulting in higher switching losses. For that, iterate in your calculations and find the conditions that yield higher switching losses and comment it in your solution.

NOTE 1: Remember that the converter is expected to always operate in ZVS which will simplify your transistor switching losses calculations. In practice, if ZVS is lost in the operation, switching losses will increase.
NOTE 2: You will need to obtain from PLECS the turn-off current of the MOSFET, which is given by the current in the magnetizing inductance.
In your answer, explain how did you find the worst-case operating conditions and indicate which simulation you got the results from.

Here we find that the worst operating conditions are at V_{max} and f_{res}. With:

$$E_{offM} = U_{DD} \cdot I_{Doff} \cdot \frac{tru + tfi}{2}$$

$$E_{onM} = U_{DD} \cdot I_{Doff} \cdot \frac{tri + tfu}{2} + Q_{rr} \cdot U_{DDD}$$

We get that $E_{onM} = 0 \Rightarrow P_{T,on}|_{nom} = 0$. This is because one of the caracterisitic of the LLC converter is to have zero voltage switching, the voltage is somehow brought down to zero before the turn-on. Hence we consider $U_{DD} = 0$ for the switch-on.

Then in order to find E_{offM}, we first need to compute:

$$tru = (U_{DD} - R_{DSon} \cdot I_{Don}) \cdot R_G \cdot \frac{C_{GD1}}{U_{(plateau)}}$$

We previously calculated $R_{DSon} = 96m\Omega$, $I_{Don} = 2.3A$, $U_{DD} = V_{max} = 50V$. We then find in the datasheet: $C_{GD1} = 60pF$, $U_{(plateau)} = 4.3V$ and $R_G = 1\Omega$ which gives us $tru = 69.5ns$ Thenwe find in the datasheet that for $I_{Don} = 15.15A$, $tfi = 9ns$. Hence for $I_{Don} = 2.3A$, we get $tfi = 1.37ns$.

This yields $E_{offM} = 4 \cdot 10^{-6}J \Rightarrow P_{T,off}|_{nom} = E_{offM} \cdot f_{res} = 0.65W$.

$P_{T,on}|_{nom} = 0$ W

$P_{T,off}|_{nom} = 0.65$ W

/ 12 pt.

Q23: EFFICIENCY

At this time, the losses of the semiconductors are known, calculate the efficiency of your LLC resonant converter under nominal operation $\eta|_{nom}$, when only semiconductor losses are considered. Please note that there will be other losses in your converter that will appear during the following stages of the design. Nevertheless, semiconductor losses are a good indication of the overall converter performance.

We first calculate

$$P_{loss,tot} = P_d + P_t + P_s = 1.272 + 0.44 + 0.65 = 2.362W$$

which then gives us:

$$\eta|_{nom} = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_{loss}} = \frac{50V}{52.362V} = 0.955$$

$\eta|_{nom} = 0.955$

/ 3 pt.

Q24: LOSS TOOL

Modify the LLC converter data input parameters in the provided loss tool in MATLAB and run it in order to acquire the losses for the different values of U_{in} and P_{out} (the loss tool already includes these values and performs the neccessary simulations). Read the comments in the code carefully to obtain valid results.

From these results, identify the nominal operating point and compare it with your results; comment deviations in case they appear. Additionally, give a brief explanation for why there are more or less losses for different operating conditions.

In Fig 11 we can see that there is apparently an issue at high input voltages with the loss-tool. As we see in Fig 12, this is because during the transient time, a very high current is induced both in the diode and in the transistor. Although the losses should only be accounted during the steady-state, the loss-tool apparently take this into account. In order to bolster this behaviour, we added a 1Ω resistor in series with the output capacitor and ogt the results in 13, which are clearly better. As in the real application, losses will be computed in steady-state, this unexpected behaviour shouldn't impact us too much.

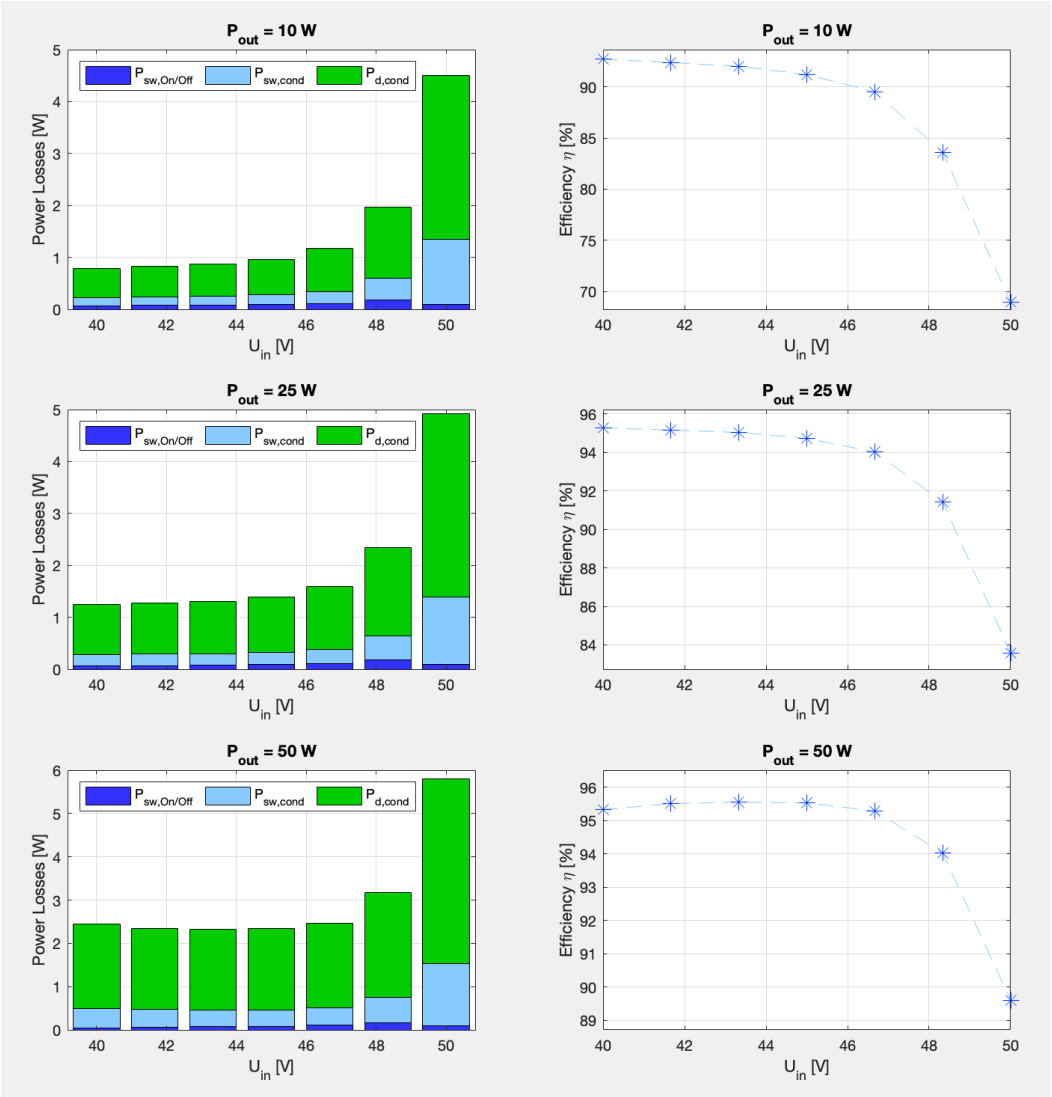


Figure 11 Semiconductor power losses and efficiencies achieved for different operating points.

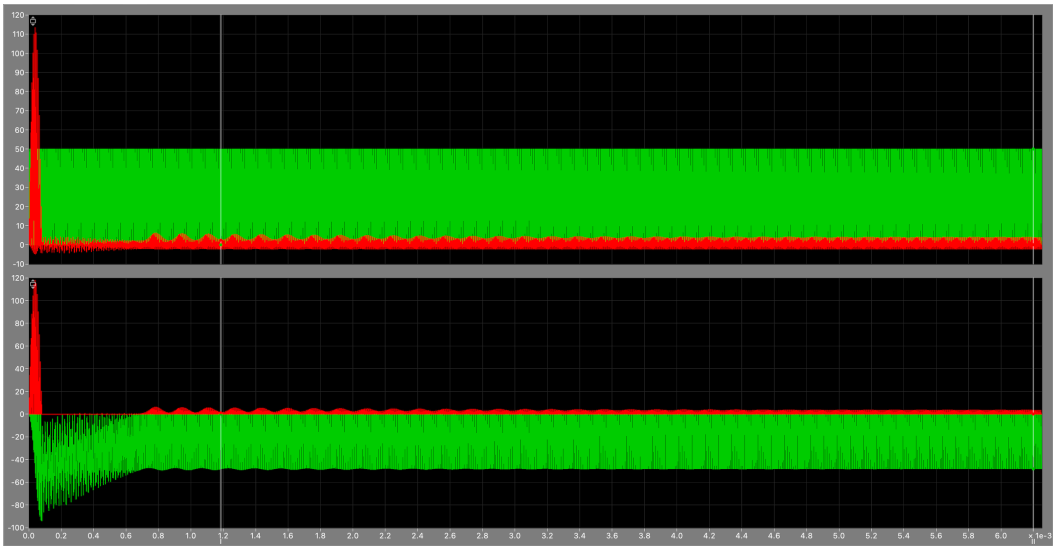


Figure 12 Current flowing in the transistor (top) and in the diode (bottom) in transient followed by Steady-State.

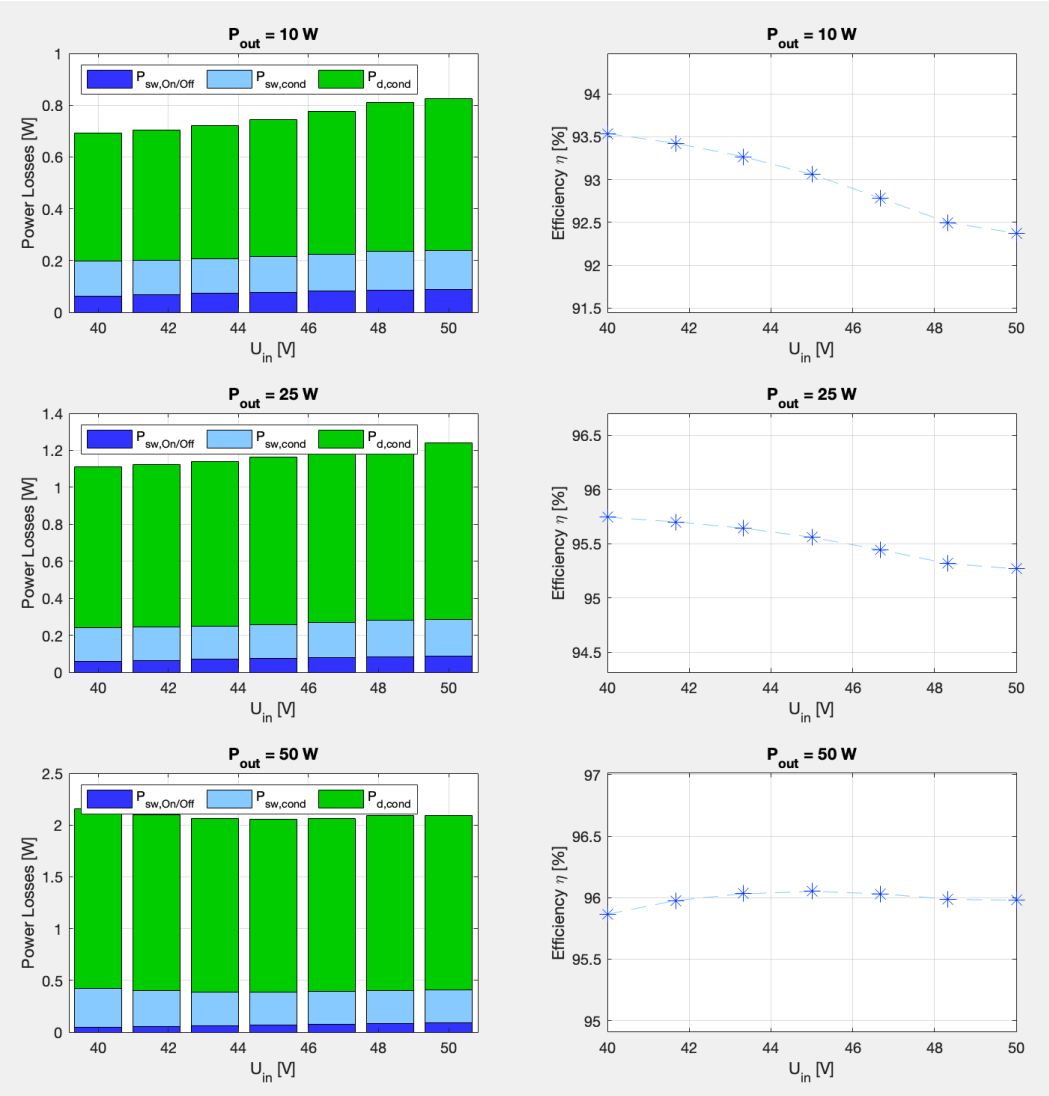


Figure 13 Semiconductor power losses and efficiencies achieved for different operating points with an added 1Ω resistor in series with the output capacitor.

/ 7 pt.

NOTE: You may consider not using a heatsink for the transistor and/or diode. Nevertheless, your decision should be based on your calculations and factors considered (i.e., temperature margin).

Q25: TRANSISTOR HEATSINK

To choose a proper heatsink, answer the following questions. For the calculations, assume a maximum ambient temperature of $\vartheta_a = 40\,^{\circ}\mathrm{C}$, whereas the semiconductor junction temperature should not exceed $\vartheta_j = 135\,^{\circ}\mathrm{C}$. Please note that there is already a thermal resistance from the junction to the case of the semiconductor.

a) Considering the output of the previous question, determine the worst case operation condition for the transistor in terms of power losses $P_T|_{wc}$.
b) Calculate the maximum allowed heatsink thermal resistance $R_{th,T,c-a}$ (where $_{c-a}$ indicates case to ambient).
c) Based on b), choose a heatsink from the selection provided in Table 4, their profile is also displayed in Fig. 14. Don't forget to highlight your selection in blue, as in Table 2.
d) Once the heatsink is selected, give the expected maximum junction temperature.

From the previous question, we find $P_T|_{wc} = 0.374891W$. Then we know that:

$$T_j = T_a + P_{loss} \cdot \sum R_{th}$$

$$R_{th,T,c-a} = R_{th,T,j-a} - R_{th,T,j-c} = 50\mathrm{K\,W^{-1}} - 1.7\mathrm{K\,W^{-1}} = 38.3\mathrm{K\,W^{-1}}$$

We can first try to see if we need a heatsink or not:

$$\vartheta_{T,j,max} = T_a + P_{loss} \cdot R_{th,T,j-a} = 313.15\mathrm{K} + 0.374891\mathrm{W} \cdot 50\mathrm{K\,W^{-1}} = 331.895\mathrm{K} = 58.74\,^{\circ}\mathrm{C}$$

This gives us a safe margin, so we don't need to add a heatsink.

$P_T\|_{wc} = 0.374891$ W	$R_{th,T,c-a} = 38.3\,\mathrm{K\,W^{-1}}$	MOSFET heatsink model No. :	$\vartheta_{T,j,max} = 58.74\,^{o}C$	/ 8 pt.

Q26: DIODE HEATSINK

Similar to the transistor, a diode heatsink has to be selected. Assuming the same thermal constraints, answer the following questions:

a) Considering the output of the Loss Tool, determine the worst case operation condition for the diode in terms of losses $P_D|_{wc}$.
b) Calculate the maximum allowed heatsink thermal resistance $R_{th,D,c-a}$.
c) Select a suitable heatsink from the selection provided in Table 4 (this time highlight it green as in Table 3).
d) Give the expected maximum junction temperature.

Similar to the transistor, we first find $P_D|_{wc} = 1.73612W$ and we also have:

$$T_j = T_a + P_{loss} \cdot \sum R_{th}$$

Here the datasheet only gives us a thermal impedence for the juction to case: $R_{th,D,j-c} = 2\mathrm{K\,W^{-1}}$. We have no information provided on the junction to air temperature, so we need to add a heatsink. We can try we the heatsink with the higher R_{th} first and scale it down if needed. We get:

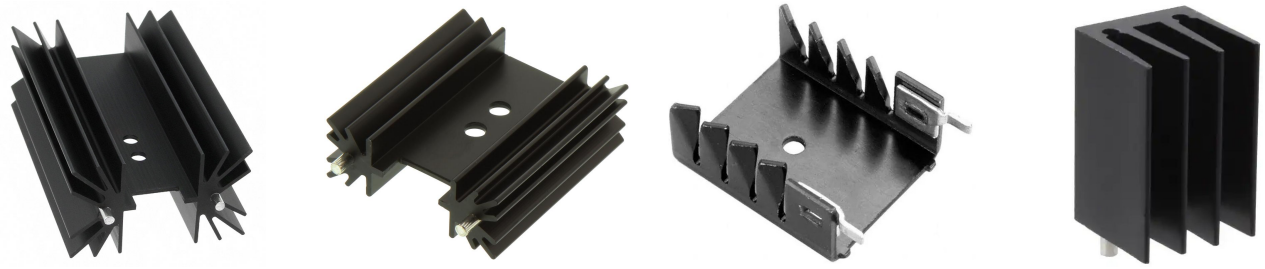
$$\vartheta_{D,j,max} = T_a + P_{loss} \cdot (R_{th,D,j-c} + R_{th,HS,c-a}) = 313.15K + 1.73612W \cdot (275.15\mathrm{K\,W^{-1}} + 16.40\mathrm{K\,W^{-1}}) = 345.095\mathrm{K} = 71.94\,^{\circ}\mathrm{C}$$

Which is well below the required $\vartheta_{D,j,max}$ so we can keep this one.

$P_D\|_{wc} = 1.73612W$	$R_{th,D,c-a} = 16.40\,\mathrm{K\,W^{-1}}$	Diode heatsink model No. : 6	$\vartheta_{D,j,max} = 71.94^{o}C$	/ 8 pt.

Table 4 List of the offered heatsinks.

No.	Manufacturer	Product	R^{th} (K W^{-1})	Figure
1	Ohmite	FA-T220-64E	3.00	14a
2	Ohmite	FA-T220-25E	4.70	14a
3	Ohmite	EA-T220-51E	7.50	14b
4	Ohmite	EA-T220-38E	10.40	14b
5	Wakefield-Vette	265-118ABHE-22	14.00	14c
6	Ohmite	E2A-T220-25E	16.40	14d



(a) Ohmite FA-T220-xxE (b) Ohmite EA-T220-xxE (c) Wakefield-Vette 265-118ABHE-xx (d) Ohmite E2A-T220-xxE

Figure 14 Available heatsinks. Images taken from the manufacturer websites.

REPORT 1 SUMMARY

Fill out the table below with your results as well as your chosen devices:

Table 5 Calculated parameter values, selected components and efficiency.

Property	Value	Unit
C_{in}	2.35	mF
C_r	271	nF
L_r	3.65	µH
L_m	18.25	µH
C_{out}	80	µF
MOSFET No.	2	–
Diode No.	3	–
$\eta\|_{nom}$	95.5	%
MOSFET heatsink No. (if present)		–
Diode heatsink No. (if present)	6	–

Total:	/ 125 pt.